Application of System-Level EM Modeling to High-Speed Digital IC Packages and PCB's

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***Abstract*— A system-level electromagnetic (EM) modeling tool combining a three-dimensional (3-D) full-wave finite-element EM-field analysis tool and a time-domain electric-circuit simulator is developed and applied to various geometries such as multilayer printed circuit boards (PCB's), signal lines embedded in a PCB or package, and split power-distribution network. Since the signal integrity is a primary concern of high-speed digital circuits, the noise distributions on various circuit planes are evaluated from the analysis. These noise distributions, often called *noice maps*, are utilized to identify the location of the major source of simultaneous switching noise (SSN). This information can eventually be adapted for optimum placement of decoupling capacitors to minimize the noise fluctuations on the various circuit planes on an entire PCB.**

***Index Terms*— Circuit simulation, decoupling capacitors, EM modeling, ground bounce, PCB, SSN, tiling.**

I. Introduction

As THE operating frequency of high-speed digital circuits (such as high-performance microprocessors) reaches up to gigahertz range, the switching noise (or ΔI noise) causes serious system malfunctions. This problem continues to grow as the clock speed of circuits increases. The speed of microprocessors become almost doubled with each new microprocessor generation, yet in the personal computer (PC) market it is unacceptable to allow the design cost to increase by a similar amount. Effective and low-cost noise reduction techniques are, therefore, necessary to minimize the impact of ΔI noise on system cost. As a result, the identification and effective suppression of the simultaneous switching noise (SSN) in the high-speed high-density digital circuits have become of critical importance.

In view of the importance of the effect of SSN, several attempts have been recently made to identify and characterize the SSN using various approximate equivalent-circuit models or experimental data [1], [2]. Further to this, with the ever increasing need for electromagnetic (EM) modeling of high-speed digital circuits and packages [3], various full-wave EM-field simulators such as the finite-element method (FEM), finite-difference time-domain (FDTD) method, and the transmission-line matrix (TLM) method are applied for more rigorous and accurate characterization of packages and high-speed digital circuits [4]–[15]. However, these full-wave tools are computationally expensive, and thus, limited to relatively simple structures.

Having realized the limitations of the equivalent circuit approaches as well as full-wave techniques on accurate and efficient modeling of digital circuits and packages, a new systematic EM-modeling methodology is proposed in this paper, and the modeling capability of the technique is proved by characterizing several practical geometries including a test vehicle. In this methodology, the seemingly contradictory goals of modeling accuracy and global analysis efficiency have been reconciled through a divide-and-conquer strategy, namely micro- and macro-modeling. The modeling accuracy is insured from the accurate full-wave EM-field simulator and the three-dimensional (3-D) FEM, and the global-analysis efficiency is achieved from the well-established time-domain circuit simulator HSPICE.

It is intended that this technique will be used to evaluate and optimize the value and placement of the decoupling capacitors for the suppression of SSN. Using this technique, the voltage distributions on the power and ground planes (noise maps) of PCB's are easily computed, and these noise maps are used to optimize the placement of decoupling capacitors as well as the pin outs of the component packages. Moreover, the driving point impedance of a whole PCB can be extracted from the voltage and current information on the noise maps. In Section II, the proposed hybrid technique is presented in detail in an effort to effectively analyze the power distribution networks of complex high-speed digital systems.

II. System-Level EM Modeling

In view of the excessive computational requirement of 3-D full-wave EM-field simulators on one hand and modeling inaccuracy of the over simplified equivalent circuit models on the other, the characterization of high-speed digital circuits and packages requires a new systematic EM-modeling strategy. Such an approach has been presented in [16] and is summarized herein for the sake of completeness. In this approach, a given PCB or package is divided into a number of smaller rectangular units—so-called "tiles"—using a nonuniform gridding algorithm. Upon completing the gridding procedure, all of the important features of the geometry, such as via holes, signal lines, or gaps have to be captured in a way that each tile contains only one kind of discontinuity element. By following

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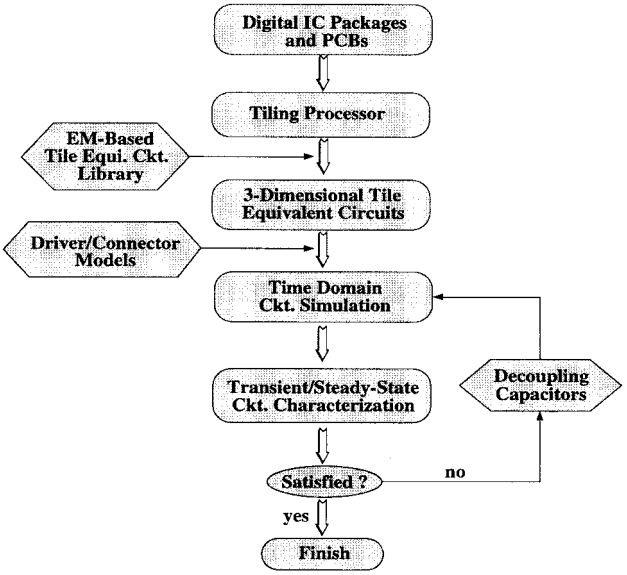

Fig. 1. System-level EM modeling of digital IC's packages and PCB's.

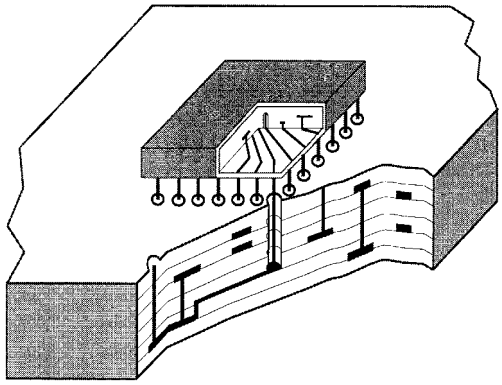

Fig. 2. Digital IC package and multilayer PCB.

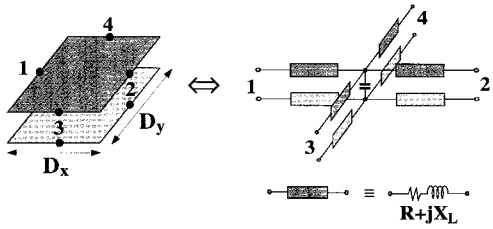

Fig. 3. Power/ground-plane tile and its equivalent circuit.

the above guideline, the accuracy of the modeling procedure is ensured due to the accurate tile equivalent circuits. The flexibility is also increased due to the standard shape of tiles. For example, if a given PCB has N power and ground pin's to be modeled accurately, the minimum required number of tiles becomes N so that each tile represents one power or ground pin. When a given PCB has multiple power, signal, and ground layers, the exactly same gridding procedure can be applied to generate 3-D tile-interconnection topology.

After the required set of tiles has been generated for a given PCB and a chip package, an appropriate lumped equivalent circuit model for each tile is derived from a rigorous EM-field simulation and appropriate microwave network theory. Specifically in this study, the 3D-FEM based on tetrahedral subdomain elements and linear edge basis functions is employed to derive accurate equivalent circuit models for vertical interconnection geometries. Since the PCB and the package have multiple power, ground, and signal pin's passing through different vertical layers, derivation of an accurate equivalent-circuit model of the vertical interconnects becomes a crucial step for efficient noise modeling.

While utilizing the FEM for vertical interconnects, microwave circuit theory has been applied to derive lumped equivalent circuit models for simpler structures, such as the power/ground plane, uniform signal lines, and gaps in the power distribution layers. After all the equivalent circuits corresponding to the defined tiles have been derived, these circuits are electrically interconnected to form a 3-D SPICE-type lumped equivalent circuit. Current or voltage sources are inserted into the network in addition to the connector configuration for the simulation of the actual situation.

The final stage of the proposed system-level EM modeling of high-speed digital integrated circuits (IC's) and packages is a time domain circuit simulation using a well-known SPICE-type simulator. The output of the simulation predicts potential fluctuations on the power and ground planes, noise maps, driving point impedance, and time domain noise signals on any power and ground pin's. These data provide valuable information for the efficient and cost-effective placement of decoupling capacitors to minimize the SSN in the circuits. The overall EM-modeling procedure for digital circuits and packages is illustrated in Fig. 1.

III. Tile Equivalent Circuits

As mentioned above, there are several distinctive tiles forming the basic building blocks of the accurate EM-modeling procedure. Power/ground plane, power/signal/ground plane, power/ground pin, and gap in the power or ground plane are the most frequently encountered form of tiles in the high-speed digital packages and interconnects, as illustrated in Fig. 2. In this section, a brief summary of the equivalent circuits for these tiles are given [16], [17].

A. Power/Ground-Plane Tile

The power distribution networks of complex high-speed digital system often consist of two conducting planes—power and ground planes—connected to system reference potentials through connector. This set of planes provides a basic tile element—a so-called power/ground-plane tile—and does not include any signal lines or vertical interconnects. Using the fact that any arbitrary current flowing on the power and ground planes can be decomposed into two orthogonal components, an equivalent circuit for the tile can be derived as a four-port network, as shown in Fig. 3.

The inductive elements on the upper and lower planes represent the effects of two orthogonal current paths on the power and ground planes, while the capacitive element at the center represents the stored electric energy between the two conducting planes. Also note that resistive elements are

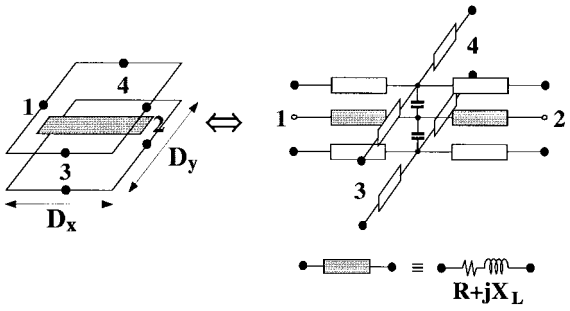

Fig. 4. Power/signal/ground-plane tile and its equivalent circuit.

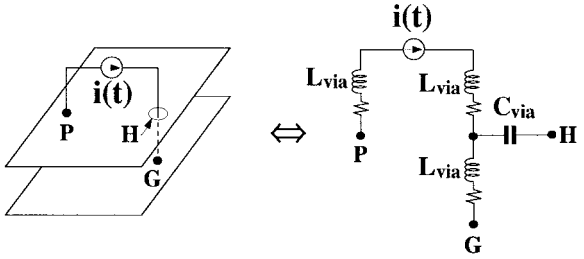

Fig. 5. Power/ground pin tile and its equivalent circuit.

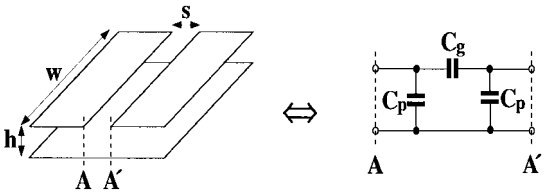

Fig. 6. Gap (slit) tile and its equivalent circuit.

inserted in series to the inductive elements to take into account the effect of conductor and dielectric losses.

The inductive and resistive elements in the lower layer corresponding to the ground plane are designed to simulate both the actual current flowing on the ground conducting surface and the resulting possible potential fluctuations. The ground plane is, therefore, no longer assumed to bear an ideal potential distribution equal to absolute zero. With this type of equivalent circuit for the power/ground-plane tile, possible SSN or ΔI noise due to the nonideal ground plane can be fully identified.

For (n, m)th tile having dimensions $D_x^{n,m}$ and $D_y^{n,m}$ in the x- and y-direction, respectively, the values of the equivalent inductive, capacitive, and resistive elements are found at the given frequency ω as follows:

$$\omega L_x^{n,m} = \frac{30\pi h}{D_y^{n,m}\sqrt{\epsilon_r}} \sin\left(\beta_g D_x^{n,m}\right) \tag{1}$$

$$\omega L_y^{n,m} = \frac{30\pi h}{D_x^{n,m}\sqrt{\epsilon_r}} \sin\left(\beta_g D_y^{n,m}\right) \tag{2}$$

$$\omega C^{n,m} = \frac{\sqrt{\epsilon_r}}{120\pi h}\left\{D_y^{n,m}\tan\left(\frac{\beta_g}{2}D_x^{n,m}\right) + D_x^{n,m}\tan\left(\frac{\beta_g}{2}D_y^{n,m}\right)\right\} \tag{3}$$

$$R = \sqrt{\frac{\omega\mu_0}{2\sigma}} \tag{4}$$

where h is the distance between the planes, ϵ_r is the dielectric constant of the material, and σ is the conductivity of the metal planes. These equations are valid when the electrical dimensions of the tile are much smaller than the wavelength of the operating frequency, i.e., $\beta_g D_{x,y}^{n,m} \ll 1$ where $\beta_g = \omega\sqrt{\epsilon_r}/c$, c is the speed of light in vacuum. In most practical high-speed digital circuits, signals contain very wide-band frequency components due to their rectangular or trapezoidal shapes having very short rise and fall edges. As a result, extracting the values of the equivalent circuit at a certain frequency point may not lead to accurate noise prediction. However, if the size of a tile is much smaller than the wavelength of significant frequency component contained in the signal (as happened in most of the examples presented in this paper), the inductive and capacitive values become frequency independent.

B. Power/Signal/Ground-Plane Tile

In many multilayer PCB's and packages, signal lines are embedded in the power and ground planes to achieve good isolation between the signal layers. The signal lines lying in the middle of the two conducting planes can be considered as a stripline having characteristic impedance Z_o. For a relatively narrow signal line, the current path along the signal line can be replaced with series inductance and resistive elements, while the interaction between the signal line and upper and lower conducting planes is modeled through the capacitive coupling as shown in Fig. 4.

The values of the series inductance and shunt capacitances for (n', m')th tile can be found as

$$\omega L^{n',m'} = Z_o^{n',m'}\tan\left(\frac{\beta_g}{2}D_x^{n',m'}\right) \tag{5}$$

$$\omega C^{n',m'} = \frac{1}{Z_o^{n',m'}}\sin\left(\beta_g D_x^{n',m'}\right) \tag{6}$$

where $Z_o^{n',m'}$ is the characteristic impedance of a stripline of width $D_y^{n',m'}$ [18]. Similar to the previous power/ground-plane tile, the above equations are valid only when the electrical size of a tile is much smaller than the wavelength of the significant frequency component contained in the signal, i.e., $\beta_g D_{x,y}^{n',m'} \ll 1$.

It is important to understand how two different types of tiles are interconnected at the interface. For example, the power/ground and power/signal/ground tiles can be interfaced by connecting the node on the top layer in one tile to the node on the top layer in the other tile, while the node in the bottom layer is connected to the corresponding node in the neighboring tile. The nodes on a signal line are not connected to neighboring nodes unless there is direct current path. As a result, the overall tile equivalent circuits form 3-D lumped-element network.

C. Power/Ground Pin Tile

In a multilayer PCB and packaging environment, the vertical interconnect such as the power and ground pin's is one of the

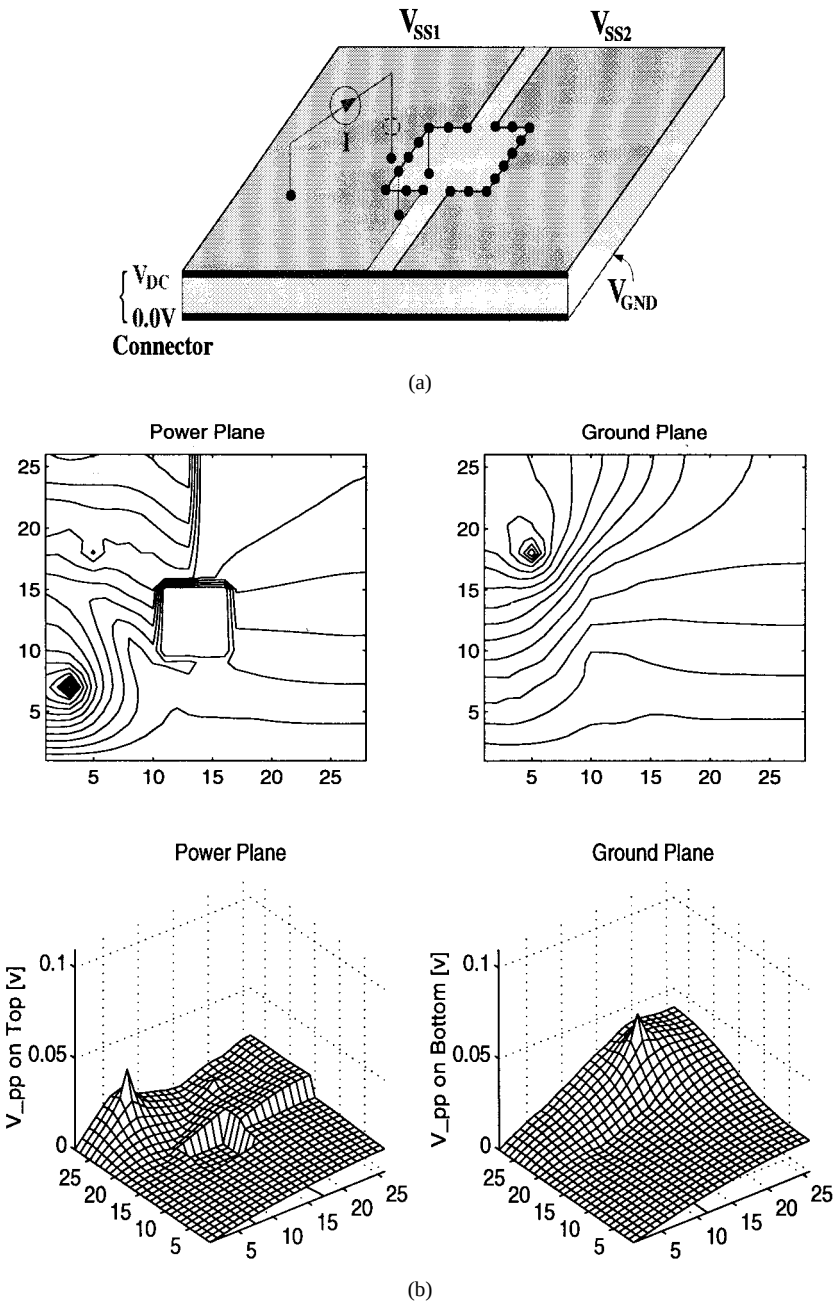

Fig. 7. Split PCB. (a) Schematics of the split PCB having 14 short-circuit pin's and large void area at the center. (b) Potential distribution on top and bottom planes.

essential and most frequently encountered circuit component. Consequently, the efficient and accurate modeling of a vertical interconnect becomes a key to successful prediction of the performance of the high-speed high-density circuits. Based on physical intuition, an equivalent circuit to this structure is devised having LC elements, as shown in Fig. 5.

The inductive elements in the circuit correspond to the lead inductance, while the capacitive element represents mutual coupling between the lead and the opening in the upper plane. The values of the inductors and capacitor can be derived from the 3-D full-wave EM-field simulators, such as the 3-D FEM and FDTD method, or analytical method [19]–[26]. Particularly, in this study, the 3-D FEM is employed to discretize the vertical interconnect into a number of subdomain tetrahedral elements, and scattering parameters are calculated over a wide frequency range. The resulting S-parameters are compared with those of the equivalent circuit to determine appropriate inductance and capacitance values [15].

In general, the lead inductance is proportional to the length of the lead h and inversely proportional to the radius of the vertical lead r, i.e., $L_{\rm via} \propto h$ and $L_{\rm via} \propto 1/r$. When there is a via pad, the total inductance of the via structure is attributed from both the pad inductance as well as from the via itself. The capacitance due to the opening in the upper plane mainly depends on h on upper and lower sides and reveals a

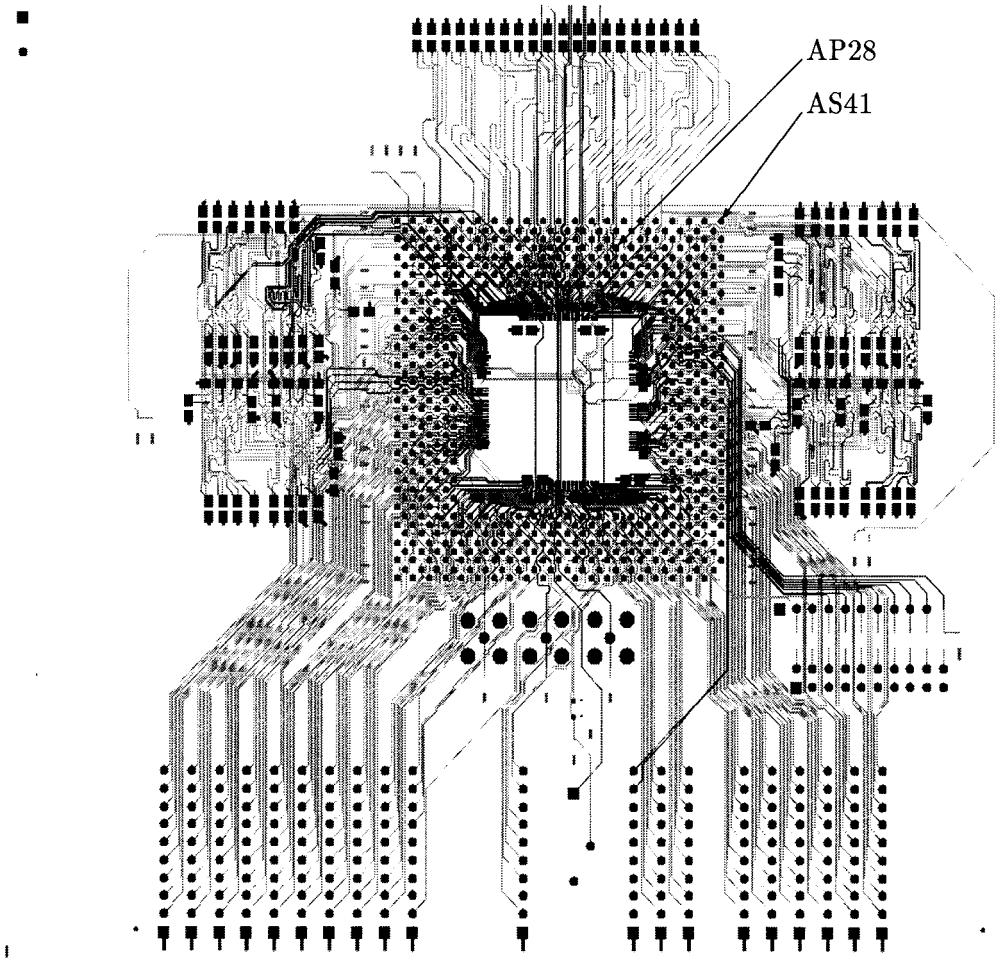

Fig. 8. Eight-layer test board layout (provided by Intel Corporation).

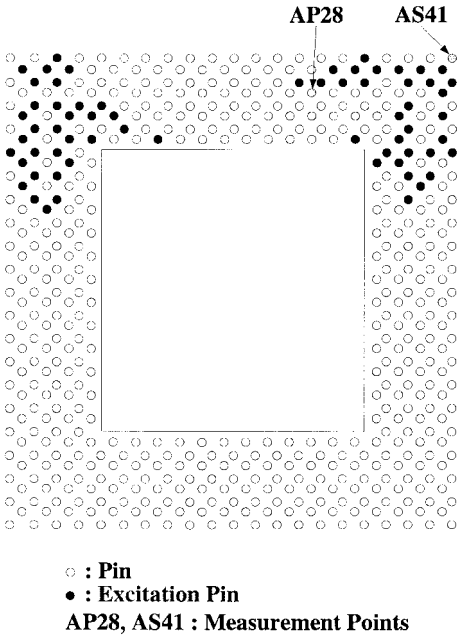

Fig. 9. Schematic of pin out and excitation pin pattern.

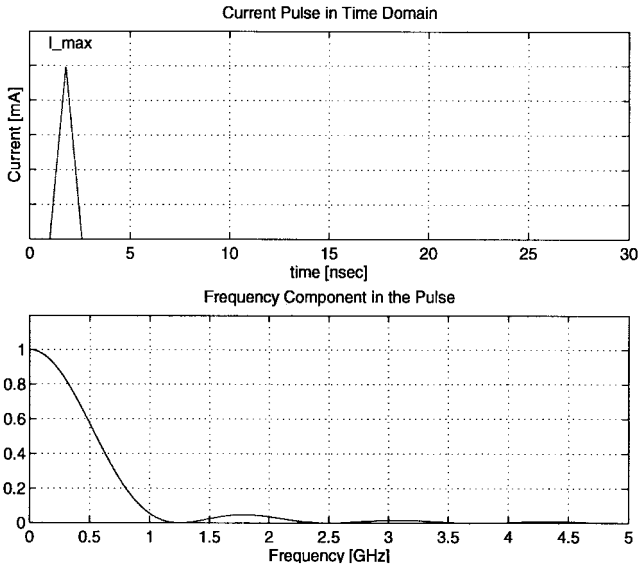

Fig. 10. Input current waveform (0.8-ns rise and fall times) and frequency components contained in the signal.

square-root dependency, i.e., $C_{\rm via} \propto \sqrt{h}$. Also, the coupling capacitance $C_{\rm via}$ sharply increases as the radius of the lead approaches that of the opening. On the contrary, as the size of the opening increases, the via capacitance decreases.

D. Gap (Slit) Tile

In many multilayer PCB structures, conducting planes are split into two or more regions to reduce overall switching noise. For the modeling of the effect of gaps in split planes, capacitive elements which correspond to the parasitic electric

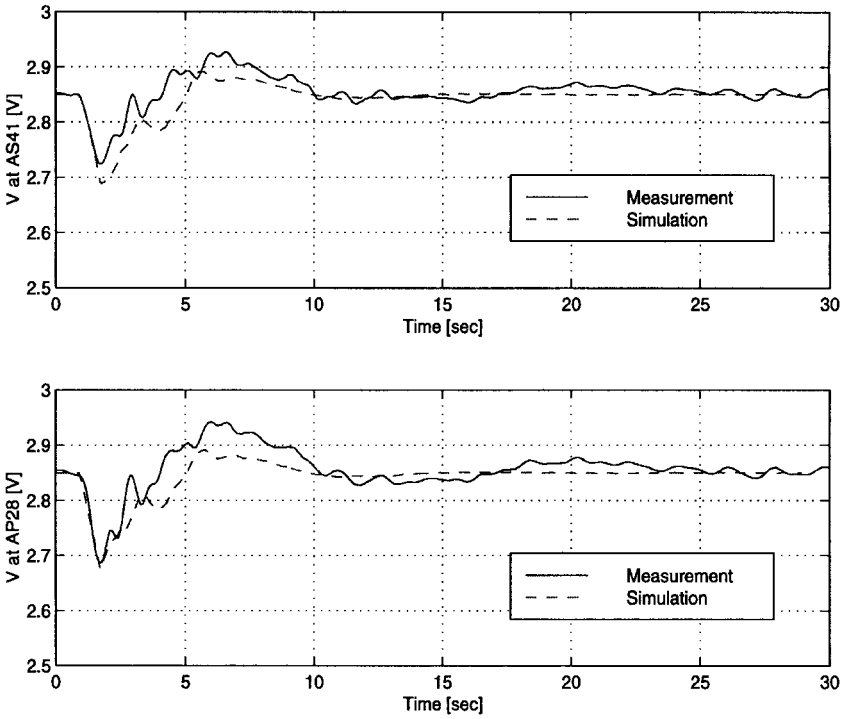

Fig. 11. Relative potential fluctuations between the power and ground planes.

energy stored in the gap region are employed, as shown in Fig. 6. Due to the discontinuity of the structure, there are no conducting currents flowing across the gap allowing the capacitive effect to be a dominant one. The gap tile is implemented by removing inductive elements from the power/ground-plane tile and instead inserting the capacitors corresponding to gap and parasitic electric fields.

Accurate values or equations of the gap and parasitic capacitances C_g and C_p can be determined from the equivalent circuit of a microstrip gap discontinuity geometry found in [27]–[31]. In this study, the following equations are derived from functional approximations and are employed by [31] for a symmetrical structure:

$$C_g = \frac{h}{2} Q_1 e^{-1.86(s/h)} \left\{ 1 + 4.19(1 - e^{-0.785\sqrt{h/w}}) \right\} \quad (7)$$

$$C_p = C_L \frac{Q_2 + (e^{-0.5978} - 0.55)}{1 + Q_2} \quad (8)$$

where

$$Q_1 = 0.04598 \left\{ 0.03 + \left(\frac{w}{h}\right)^{1.23} \right\} (0.272 + 0.07\epsilon_r)$$

$$Q_2 = 0.107 \left[\frac{w_2}{h}\right] + 9\left(\frac{s}{h}\right)^{3.23} + 2.09\left(\frac{s}{h}\right)^{1.05} \left(\frac{1.5 + 0.3\,w/h}{1 + 0.6\,w/h}\right).$$

The equation of the terminal capacitance C_L for an open circuit with conductor width w can be found in [32]. The normalized terminal capacitance C_L/w reduces with decreasing w/h and approaches a value of $C_{L,\infty}/w \simeq 0.012 + 0.0039\epsilon_r$ in picofarad/millimeter for large conductor width $w/h \geq 1$. In (7) and (8), C_g is in picofarad and h in millimeter. The above equations are valid for the ranges $0.1 \leq w/h \leq 3.0$ and $0.2 \leq s/h \leq \infty$, for substrate permittivities $6.0 \leq \epsilon_r \leq 13$, and in the frequency range $0 \leq h \cdot f \leq 12$ GHz · mm. For a substrate having ϵ_r outside of the valid region, the capacitances can be estimated with $C(\epsilon_r) = C(9.6) \cdot (\epsilon_r/9.6)^{0.9}$. In our modeling procedure, the above constraints are carefully enforced during the tiling procedure unless otherwise specified.

It can be seen that C_g and C_p approximately increase linearly with ϵ_r for constant w/h and s/h. Note that for large values of s/h, C_g approaches to zero, corresponding to an open circuit. On the other hand, as s/h approaches to zero, the value of the parasitic capacitances C_p becomes smaller. When the gap spacing s becomes much larger than the tile-width w, the gap tile is modeled as an open circuit having only parasitic capacitance C_p.

IV. Numerical Results

In this section, by using the proposed system-level EM-modeling technique, several interesting and practical geometries are modeled to characterize SSN on multilayer PCB and packaging environment. Firstly, the effect of splitting the top plane into two regions is modeled, and resulting potential fluctuations on top and bottom planes are computed. Secondly, a test vehicle having eight layers of power, signal, and ground planes is fully modeled and compared with the voltage measurement on various places. The effects of signal lines embedded between the power and ground planes are also closely examined with an actual buffer model.

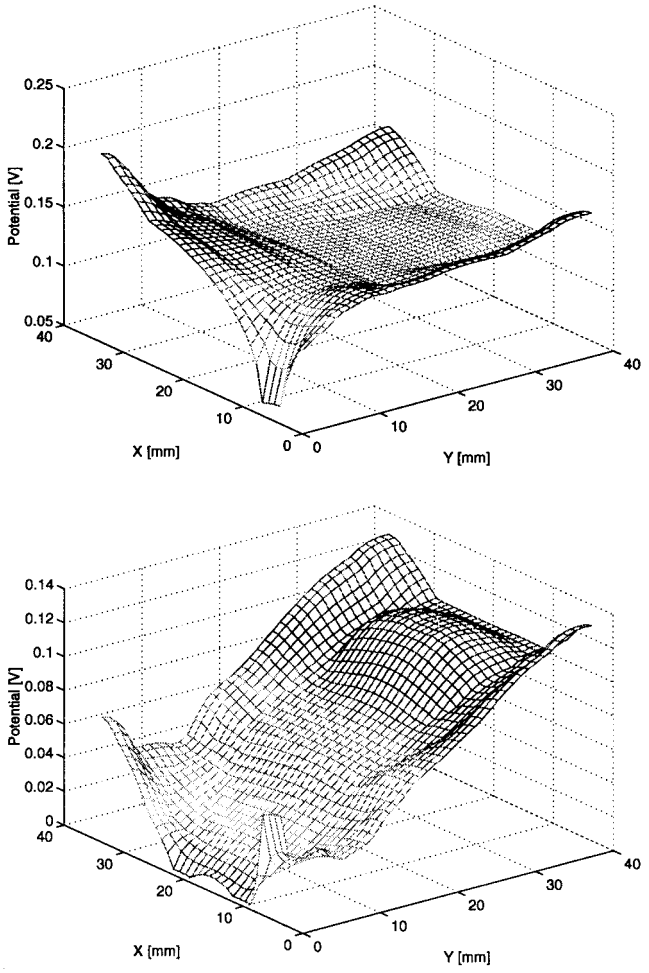

Fig. 12. Noise maps (peak-to-peak potential fluctuations) on the power and ground planes.

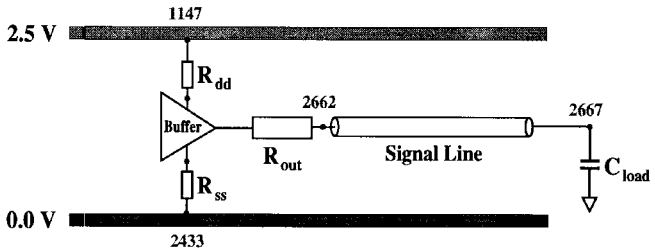

Fig. 13. Cross-sectional view of a signal line terminated with capacitive load. Top and bottom planes: 175 mm × 184 mm. Length of the signal line = 5.0 mm. $C_{\rm load} = 18$ pF, $R_{dd} = R_{\rm gnd} = R_{\rm out} = 0.001\ \Omega$.

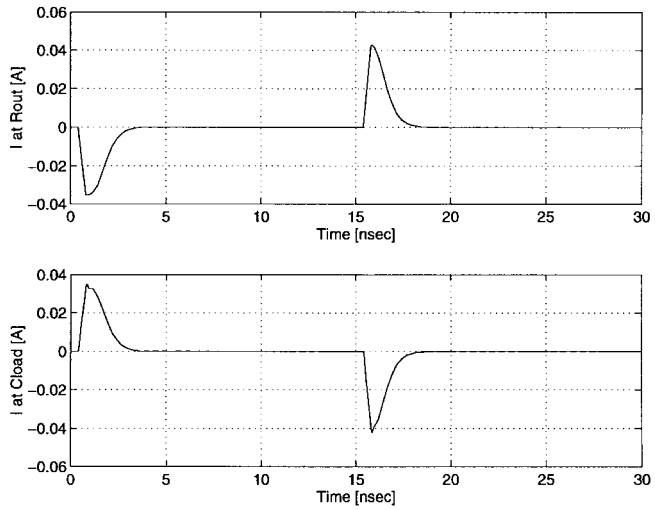

Fig. 14. Simulated current waveforms at the output resistor ($R_{\rm out}$) and capacitive load ($C_{\rm load}$).

A. Split PCB

In this section, a 64 mm × 64 mm PCB is modeled with 26 × 28 nonuniform tiles. As shown in Fig. 7(a), the upper plane is split into two regions. The gap spacing and the thickness of the substrate are 2.54 and 0.2 mm, respectively, and the relative dielectric constant ϵ_r of the material is 2.5. 14 short-circuit pin's modeled as inductive elements are also placed at the central region to reduce the overall noise levels on top and bottom planes. For the excitation of the structure, one current source is supplied as shown in Fig. 7(a) and the input current waveform is designed to have 100-mA magnitude and 0.5-ns rise and fall time. In view of high-frequency components contained in the signal, the equivalent circuits are extracted at $f = 2$ GHz. Also, a connector providing 2.5 and 0.0 V on the top and bottom planes is placed at the front side of the PC board.

After the EM modeling of the overall geometry, an efficient circuit simulation is exercised to derive the potential distribution on the top and bottom planes. After 10 ns of time-domain simulation, the peak-to-peak values at each grid point on the top and bottom planes and the corresponding noise maps are derived, as shown in Fig. 7(b). The maximum noise on those planes are 47.7 and 66.7 mV, respectively, at the position of the current source. As can be observed, there is clearly a potential difference between the top two planes due to the 2.54-mm gap region revealing effective noise immunization of splitting PCB's.

B. Eight-Layer Test Board

For the proof of the accuracy as well as efficiency of the proposed approach, an eight-layer test vehicle, shown partly in Fig. 8, is fully modeled and the noise level is measured under a controlled environment. To minimize the measurement errors and uncertainties, multiple CMOS drivers are simultaneously switched, as shown in Fig. 9, and the voltage differences between the power and ground planes at various locations are measured and compared with the modeled results. For accurate and efficient modeling, the test PCB is discretized into a number of tiles (34 × 37 nonuniform tiles) and 64 ideal triangular current sources are simultaneously excited between the power and ground pin's at various places. Those 64 sets of power and ground pin's form two groups (32 in each group) and each aggregated current source group is located in the upper left and right corner of the chip area, as shown in Fig 9. For simulation purposes, ideal current sources having 0.8-ns rising and falling times are used and its frequency

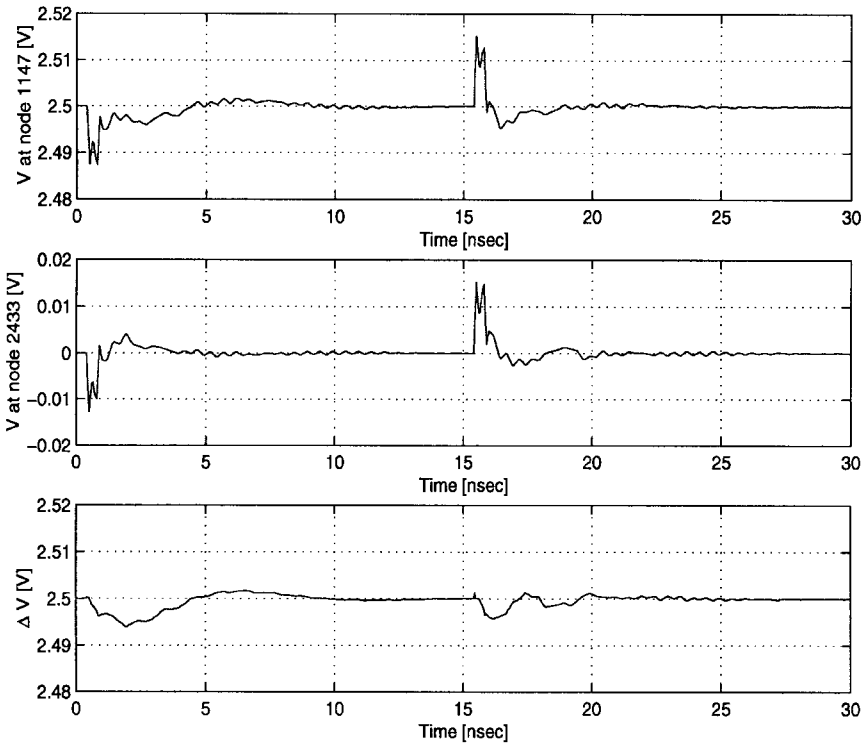

Fig. 15. Simulated potential fluctuations on the power (node 1147) and ground plane (node 2433) with a signal line terminated with capacitive load. The voltage difference between the power and ground plane is denoted as ΔV, which is indicating a noisy power-distribution layer.

content are shown in Fig. 10. The triangular shape of the input currents with 15-mA magnitude is estimated from the actual CMOS driver. Note that the Fourier components in the input current signal span up to near gigahertz range due to the fast edge rates.

As shown in Fig. 11, simulation has been performed and the voltage waveforms at two different locations denoted as $AS41$ and $AP28$ are compared with the measurement data. These measurement points are located in the upper right corner of the chip area. The overall simulation, including tiling procedure and circuit simulation, took about 3 h on an HP 9000/735 workstation with 130-Mbytes memory usage. As can be observed from the voltage waveforms, the measurement and simulation results reveal very good agreement even for the small details. This agreement supports the validity and effectiveness of the proposed system-level EM-modeling technique. In addition, noise maps (peak-to-peak values) on the power and ground planes are illustrated in Fig. 12 and the maximum values on the power- and ground-plane noise maps are found as $V_{pp}^{\rm pwr} = 205$ mV and $V_{pp}^{\rm gnd} = 134$ mV, respectively. Note that the minima in the noise maps correspond to the connector locations which provide constant potentials.

C. Signal Lines

After the verification of the accuracy of the proposed modeling procedure, in this section the effects of nonlinear drivers and signal lines terminated with capacitive loads are simulated, using the power/signal/ground-plane geometry designed with one signal line, as depicted in Fig. 13. The geometrical factors of the PCB are similar to those of the previous test vehicle and the signal line is placed in the middle of the substrate. The buffer model used in this study has three terminals, such as V_{dd}, $V_{\rm gnd}$ and output, and those are connected to 0.001 Ω resistors, R_{dd}, $R_{\rm gnd}$, and $R_{\rm out}$, respectively, while an input excitation having 0.4-ns switching time is embedded in the driver model. In the buffer model, p- and n-channel CMOS look-up tables are used to simulate the actual transistor characteristics.

After 30-ns transient analysis, the current waveforms at the output resistor $R_{\rm out}$ and capacitive load $C_{\rm load}$ are examined first, as illustrated in Fig. 14. As can be identified from the current waveforms, there is a slight reflection at the beginning of the signal line due to the impedance mismatch and the phase of current at the capacitor is reversed. Also, Fig. 15 shows the voltage waveforms on the power and ground planes revealing ground bounce caused from a nonideal ground plane. The potential difference between the power and ground planes can be considered as noise if that is not constant and equal to the connector potential, which in this case is 2.5 V.

V. Conclusions

This paper has presented a system-level methodology for the modeling and analysis of digital IC packages and PC boards. In this methodology, the seemingly contradictory goals of modeling accuracy and global analysis efficiency are reconciled through a divide-and-conquer process. Accuracy is insured by performing detailed EM-field analysis on appropriately

chosen small sections of the PCB and package to create lumped electrical equivalent circuit models. These models are subsequently combined with models for chip current drivers and package leads to produce an electrical simulation model for the PCB power distribution subsystem. A circuit simulator is then used to exercise this model under a variety of current excitation conditions to yield noise maps that indicate the variation in power and ground potential as a function of location on the PCB.

The validity and efficiency of our proposed system-level EM-modeling methodology have been proven through several different experiments including a split PCB and an eight-layer test vehicle. The theoretical results for the test board show very good agreement with the measurement data obtained from the actual board under control environment. Owing to the flexibility of the modeling method, voltage and current waveforms at arbitrary locations can easily be made visible. Furthermore, the effects of signal lines, gap in the conducting plane, and decoupling capacitances can be quantified.

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